ANALOG INTERFACE LITERATURE PACKAGE

POLYMORPHIC SYSTEMS
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A/D D/A INTERFACE

PRELIMINARY
Table of Contents

1. Assembly and Operation Instructions

1.1 Component Check

This analog interface kit comes equipped in standard form with one unipolar analog output (0-10V). A bipolar option (-5 ot 5V) is available, as well as an additional output channel. Thus, there are several variations on the standard kit, which are accomodated by grouping the components in bags; different bag combinations go with each option. There are six different bags, numbered Ø through 5. Depending on the option chosen, the number of each bag type enclosed follows this table:

PART #	CONTENTS
ADA/1K	Analog- Circuit board, literature, bags #Ø, #1, #2
ADA/2K	Analog- Circuit board, literature, bags #Ø, #1, #3, & 2 bag #2's
ADA/1BK	Analog- Circuit board, literature, bags #Ø, #1, #2, #3
ADA/2BK	Analog- Circuit board, literature, bags #Ø, #1, #3, #5, & 2 bag #2's
ADA/1A	Assembled ADA/1S, literature
ADA/2A	Assembled ADA/2S, literature
ADA/1BA	Assembled ADA/1BS, literature
ADA/2BA	Assembled ADA/2BS, literature
ADA/SK	Analog Bag #4
ADA/1KS	Analog- Circuit board, literature, bags #Ø, #1, #2, #4
ADA/2KS	Analog- Circuit board, literature, Bags #Ø, #1, #4, & 2 bag #2's
ADA/1BKS	Analog- Circuit board, literature, bags #Ø, #1, #2, #3, #4
ADA/2BKS	Analog- Circuit board, literature, bags #Ø, #1, #3, #4, #5, & 2 bag #2's
ADA/1CO	Analog Bags #2, #5
ADA/BO	Analog Bag #3

Check to see that you have received the correct number of each type of bag. Check also to see that each bag contains the correct components as listed on the following page.

ANALOG INTERFACE PARTS LIST

BAG # Ø Integrated circuits

Qty	P/N
1	78MGT2
1	79MGT2
1	DM8131
2	N8T97 or DM8097 or SN74367
1	74LS138
4	LM319
1	74LS20
2	74LS04

BAG #1

1	LM340T-5.0 or MC7805P
1	Heat sink
6	10 µf tantalum capacitors
12	0.1 µf Disc capacitors
15	2200 ohm ¼W 10% resistors (red-red-red)
1	7.15K ohm 1/8W 1% resistor (7151F)
1	8.45 ohm 1/8W 1% resistor (8451F)
1	11.3K ohm 1/8W 1% resistor (1132F)
1	6-32 screw
1	6-32 nut
1	6-32 lockwasher
1	solder
1	12" #18 wire
1	spaghetti

BAG #2

1	89 PR 10K ohm trimpot
1	89 PR 200 ohm trimpot
1	4.75K ohm 1/8W 1% resistor (4751F)
1	DAC 100-CCT1
1	MC1741 SCP1
2	P8212 or SN74S412N
1	16 pin I.C. socket

BAG #3 Bipolar option

1	1N4580
1	2200 ¼W 10% resistor (red-red-red)
2	89 PR 500 500ohm trimpot

BAG #4 Socket kit

4	24 pin sockets
7	16 pin sockets
7	14 pin sockets
2	8 pin sockets
1	14 pin dip switch

BAG #5

Qty	P/N
1	74123
1	22K ¼W 10% resistor (yellow-violet-orange)
1	10K ¼W 10% resistor (brown-black-orange)
2	.001 µf Disc capacitors

1.2 Assembly Instructions

All components will be loaded from the TOP of the board, which is viewed when the 100 pin bus connector is oriented down and the 44 pin analog interface connector is on the upper right. This is verified by reading the word "TOP" etched on the board about half way up the right hand edge. When viewed in this orientation, all the dual-in-line packages (DIP's), except one (IC7), have pin #1 on the left hand side. That is, DIP's which are or oriented vertically have their first pin at the upper left and DIP's which are horizontal have pin #1 at the lower left.

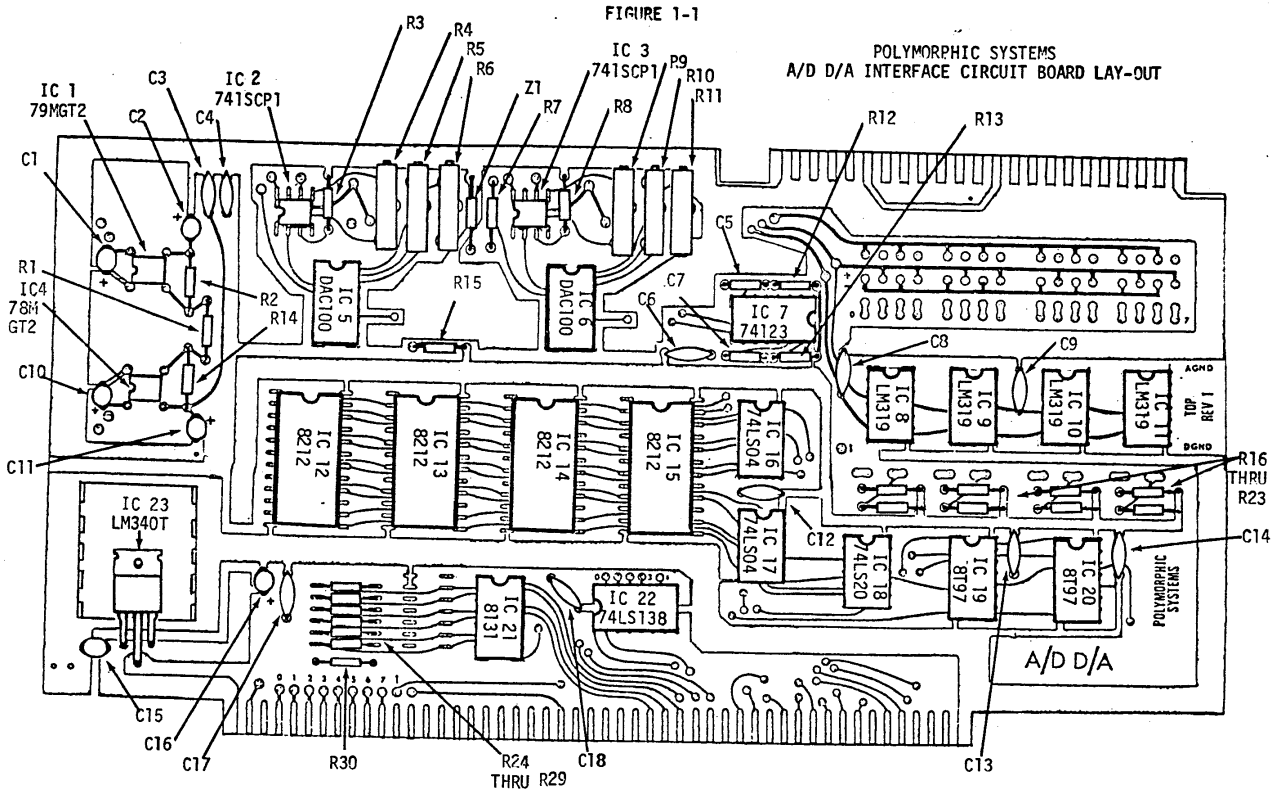
Insert the following DIP's into the board by referring to figure 1-1 for each device location. Solder all pins on each device from the bottom of the board, being careful not to create solder bridges to adjacent pins or traces. If you are not familiar with DIP insertion and soldering techniques, refer to the enclosed sheet on DIP handling. Note that IC's 2, 5, 12 and 13 are only included with the 2 output options.

1.2.1 Integrated Circuit Installation

CHECK	IC #	TYPE	FUNCTION
( )	1	79MGT2	Negative voltage regulator
( )	2 *	741SCP1	Operational amplifier
( )	3		
( )	4	78MGT2	Positive voltage regulator
( )	5 *	16 PIN Socket	Socket for DAC
( )	6		
( )	7 *	74123	Dual one-shot
( )	8		
( )	9		
( )	10	LM319N	Dual analog comparators
( )	11		
( )	12 *		
( )	13 *	8212, 74S412	8-bit I/O ports
( )	14	or equivalent	
( )	15		

* supplied with 2 output option only

FIGURE 1-1


POLYMORPHIC SYSTEMS
A/D D/A INTERFACE CIRCUIT BOARD LAY-OUT
IC 1 79MGT2
IC 2 741SCP1
IC 3 741SCP1
IC 4 78H GT2
IC 5 DAC100
IC 6 DAC100
IC 7 74123
IC 8 LM319
IC 9 LM319
IC 10 LM319
IC 11 LM319
IC 12 8212
IC 13 8212
IC 14 8212
IC 15 8212
IC 16 74LS04
IC 17 74LS04
IC 18 74LS20
IC 19 8T97
IC 20 8T97
IC 21 8131
IC 22 74LS138
IC 23 LM340T
R1
R2
R3
R4
R5
R6
Z1
R7
R8
R9
R10
R11
R12
R13
R14
R15
R16 THRU R23
R24 THRU R29
R30
C1
C2
C3
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
C17
C18
AGND
+5V
+12V
-12V
BGND
POLYMORPHIC SYSTEMS
A/D D/A

1.2.1 Integrated Circuit Installation (Cont.)

CHECK	IC #	TYPE	FUNCTION
( )	16	74LS04	Hex inverter/buffer
( )	17		
( )	18	74LS20	Dual 4 input NAND gate
( )	19	8T97 or 8097	Tri-state drivers
( )	20	or 74367	
( )	21	DM8131	6 input comparator
( )	22	74LS138	Decoder

( ) The last integrated circuit, IC 23, is a 780507 or 7436 5 Volt regulator. It is not in a dual-in-line package but has a metal tab and three leads. Place the hole in the metal tab over the hole in the large heat sink area on the lower left of the circuit board. Orient the three leads downward over the three holes shown in figure 1-1 and note where to bend them to go through. Bend them with small pliers, and check to see that when the three leads go through the board the mounting holes line up. Then, insert the 6-32 screw from the bottom of the board; place the heatsink over the screw from the top and insert the regulator leads into the board while the tab slips over the machine screw. Use the lockwasher and nut to secure the regulator and heatsink to the board. Solder the three leads and trim.

1.2.2 Capacitor Installation

( ) Insert 10μF tantalum capacitors C1, C2, C10, C11, C15 and C16 as shown in figure 1-1. Note the orientation of each capacitor from the + mark on the drawing and the board. Bend back each lead as you insert the capacitors, solder all of them and trim.

( ) Insert .1μF disc capacitors C3, C4, C6, C8, C9, C12, C13, C14, C17 and C18 as shown. Solder and trim.

( ) If you have the 2 output option, insert .001μF disc capacitors C5 and C7 as shown in figure 1-1. Solder and trim.

1.2.3 Resistor Installation

( ) Insert 2.2K resistors (red-red-red) R15 through R30 as shown in figure 1-1. Solder and trim.

( ) Insert 7.15K 1% resistor R1 as shown. Solder and trim.

( ) Insert 11.3K 1% resistor R2 as shown. Solder and trim.

( ) Insert 8.45K 1% resistor R14 as shown. Solder and trim.

( ) Insert 4.75K 1% resistor R8 as shown. If you have the 2 channel option, insert the corresponding resistor R3. Solder and trim.

( ) If you have the bipolar option, insert 2.2K resistor (red-red-red) R7 as shown. Also insert zener diode Z1 (1N4580) next to R7 as shown. Solder and trim.

( ) If you have the 2 channel option, insert 47K resistor (yellow-violet-orange) R12 and 10K resistor (brown-black-orange) R13 as shown. Solder and trim.

( ) Insert 200Ω trimpot R10 as shown. If you have the 2 channel option, insert the corresponding resistor R5. Solder and trim.

( ) If you have the bipolar option, insert the 500Ω trimpot R11 as shown. If you have a unipolar output, insert the 10K trimpot R9. If you have the 2 channel option, insert the corresponding resistor: 500Ω at R6 for bipolar or 10K at R4 for unipolar.

1.3 Operation Instructions

Section 1.2 completes the basic assembly of the board, but there are several remaining connections to be made before the interface can be used. These include output port address selection, interrupt priority selection and configuration of the analog comparator inputs and outputs.

1.3.1 Address Selection

The analog interface board interacts with the Altair bus as four output ports and one input port (see section 2). The 8080 allows 256 input or output ports to be addressed by an eight bit byte. The four output ports are arranged so that the six most significant bits of the port address are jumper selectable, while the last two bits determine which of the four ports is addressed. If the six jumper selected bits are the six most significant bits of an output instruction, then one of the 8212's (IC12, 13, 14 or 15) will latch the data off the data out bus. If the least significant bits are ØØ, then IC12 will take the data, which then forms the most significant 8 bits of analog output #1. If the port address ends in Ø1, then IC13 takes the data. The 2 least significant bits of this data then become the two least significant bits of channel 1. If the port address ends in 1Ø, then IC14 takes the data as the most significant byte of channel 2. Channel 2 is the reference channel for the analog comparators, which is why it is inserted when only one channel is desired. If the output address is 11, then IC15 latches the two least significant bits of channel 2 and the six digital control outputs off the data bus. The input port reflects the state of the eight analog comparators, and responds upon an input instruction addressed by the six jumper bits followed by ØØ.

The address selection jumper area is located in the lower left hand region of the board, adjacent to IC21. Each of the six most significant bits of the address are tied with a resistor to +5V, so that they are normally in the binary state 1. Any or all of them may be jumpered to ground to put them in the binary state Ø. Note the two rows of pads to the left of IC21 (see Fig. 1-2). These pads are on a dual-in-line spacing so that a DIP

1.3.1 Address Selection (Cont.)

switch may be used for address selection , if desired. Normally the address line on the right may be jumpered directly to the grounded pads on the left, with the bit sequence as shown in figure 1-2.

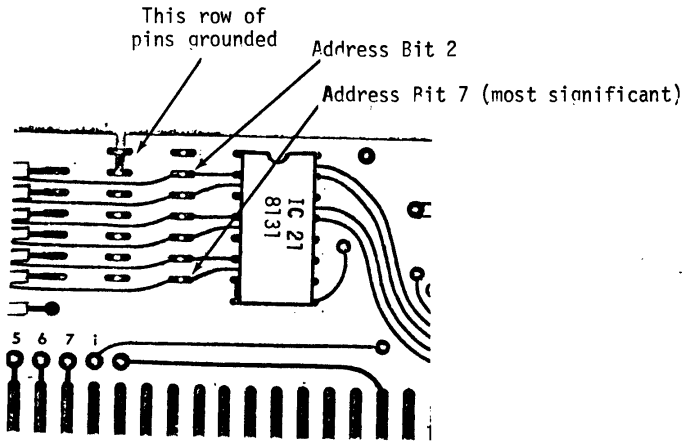


Figure 1-2

1.3.2 Comparator Input Configuration

The eight analog comparators may be arranged for null detection, level sensing, or analog conversion depending on the configuration of their inputs. Observe the region in the upper right hand corner of the board (shown in figure 1-3). This area provides for connection of the comparator inputs to the analog inputs, the analog output or to a resistor divider between the supply voltages or ground. Thus one can compare the input to the output (for A/D conversion) or to any fixed voltage (for level or null detection). See section 3.3 for typical application of these features.

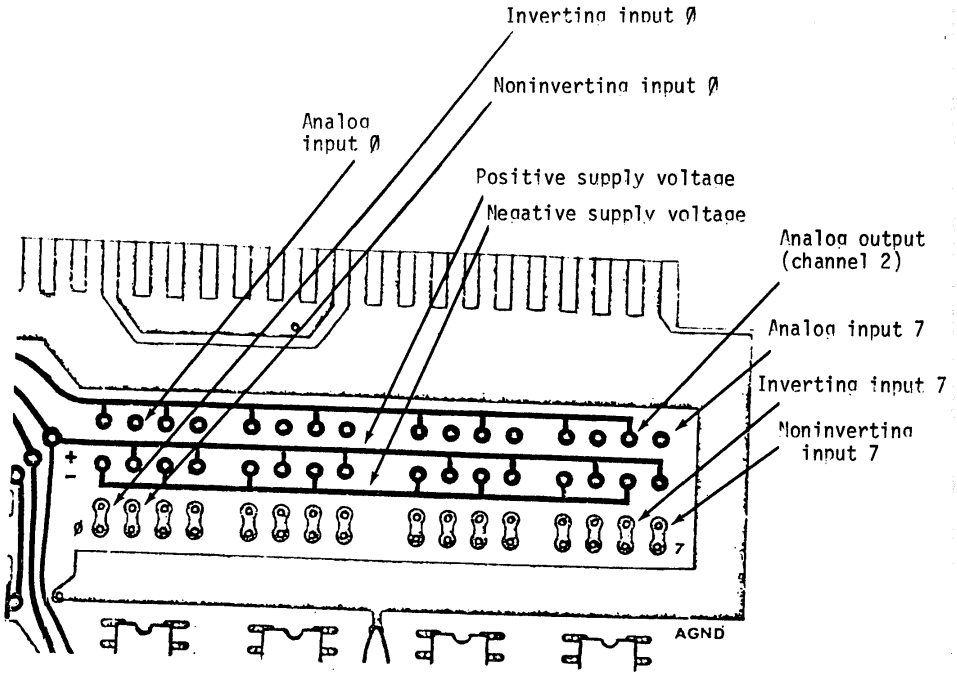


Figure 1-3

1.3.3 Comparator Output Configuration

The outputs of the comparators are arranged as shown in Figure 1-4. The IC outputs are open collector: hence the pullup resistors R16 through R23. This is done so that an interrupt can be generated by any output or any combination connected together (logical AND). Thus when each comparator on the interrupt sense line has the voltage on its non-inverting input higher than that on its inverting input, an interrupt is generated. But if this condition is reversed on any one of these comparators, then its output will ground the interrupt sense line.

After an interrupt is generated, the interrupt service routine must access IC15 to clear the interrupt request flip-flop. This is accomplished by an output instruction to the six jumper bit address followed by 11 (binary).

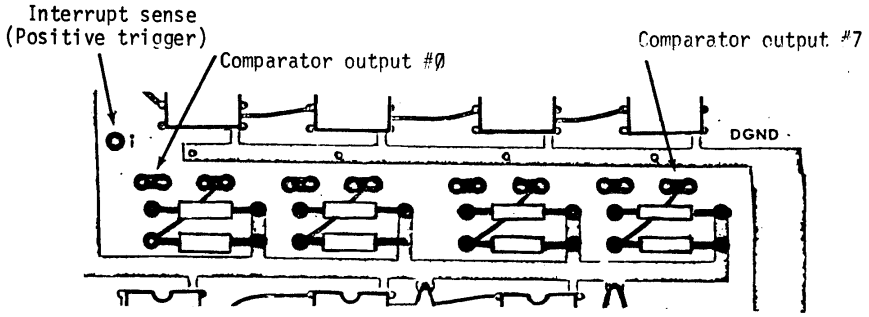


Figure 1-4

1.3.4 Interrupt Priority Selection

If the interrupt sense input is used as described in the previous section, then the interrupt priority must be selected for the output of the interrupt flip-flop. The interrupt output is assigned a priority Ø through 7 by jumpering it to the appropriate bus line as shown in Figure 1-5 (see the Altair literature for a complete description of the interrupt system).

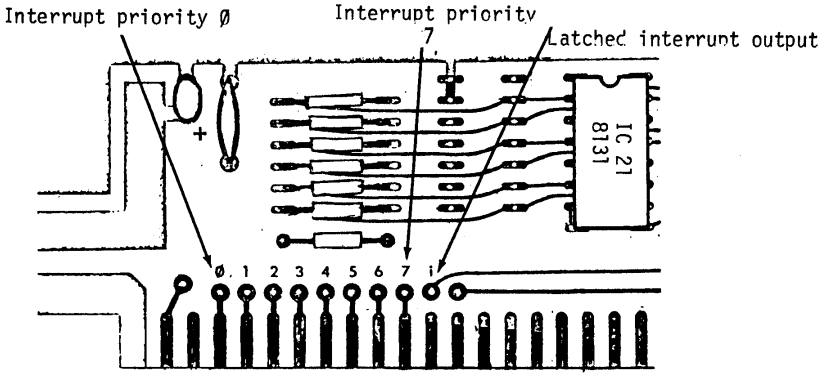


Figure 1-5

1.3.5 Output Strobe One-Shot

Included with the 2 channel option is a dual one-shot (IC7) which can be triggered by an output instruction. This is useful in certain applications where the output can be disabled during the transition from one output state to another. For example, when the analog outputs are used to drive the x and y channels of an oscilloscope, the Z axis (beam intensity) can be driven by the one-shot output to blank the screen during the transition from point to point. The components supplied with the 2 channel option cause this control output to go low for approximately 13µs starting 3µs after the trigger port is addressed. The trigger port can be any one of the four output ports, and is selectable by jumpering as shown in Figure 1-6.

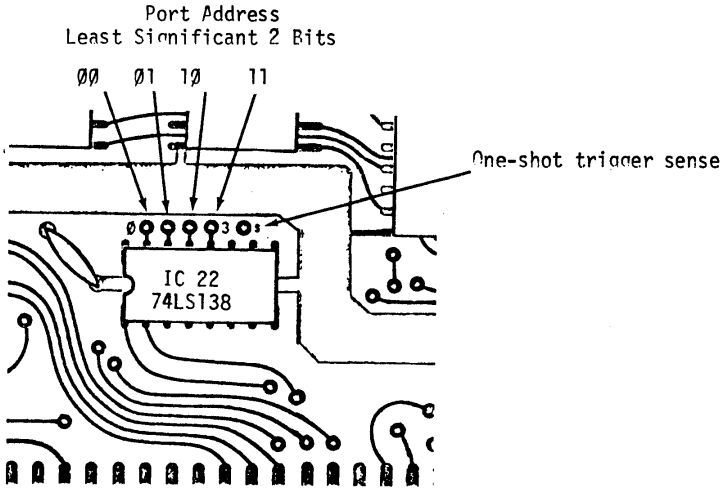


Figure 1-6

1.4 Noise Control

There are several provisions on the analog interface which are designed to limit the introduction of digital noise into the analog circuitry. The interior of the Altair is an extremely noisy environment, so every effort has been made to isolate the analog circuitry. Most importantly, the digital and analog grounds are kept separate so that they may be referenced together at a single point. Good grounding rules must be followed, with the two grounds separate except at the reference point. The board has the two grounds tied together by a small trace at the extreme right hand edge of the board. This trace is easily cut so the grounds can be referenced at the sensor or at the Altair power buss terminal if noise is a problem in your application, Jumper pads are provided to replace the cut trace if you later desire. DAMAGE MAY RESULT TO THE DAC'S IF THE GROUNDS ARE NOT REFERENCED TOGETHER, so be sure that if you cut the trace, you then reference the grounds at some other point.

Provision is also made so that an entirely separate power supply can be used for the analog section. The ±16 V Altair power is connected to the positive and negative voltage regulators by traces which may be cut, if desired. The unregulated inputs to these voltage regulators have pads to re-connect to the Altair power, as well as being brought out to the analog interface connector. Thus an external supply can drive the analog section as an alternative to the Altair power supply, which is sufficient for most applications. The reconnection jumpers are shown in figure 1-7.

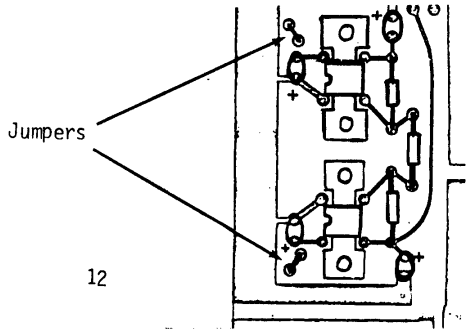
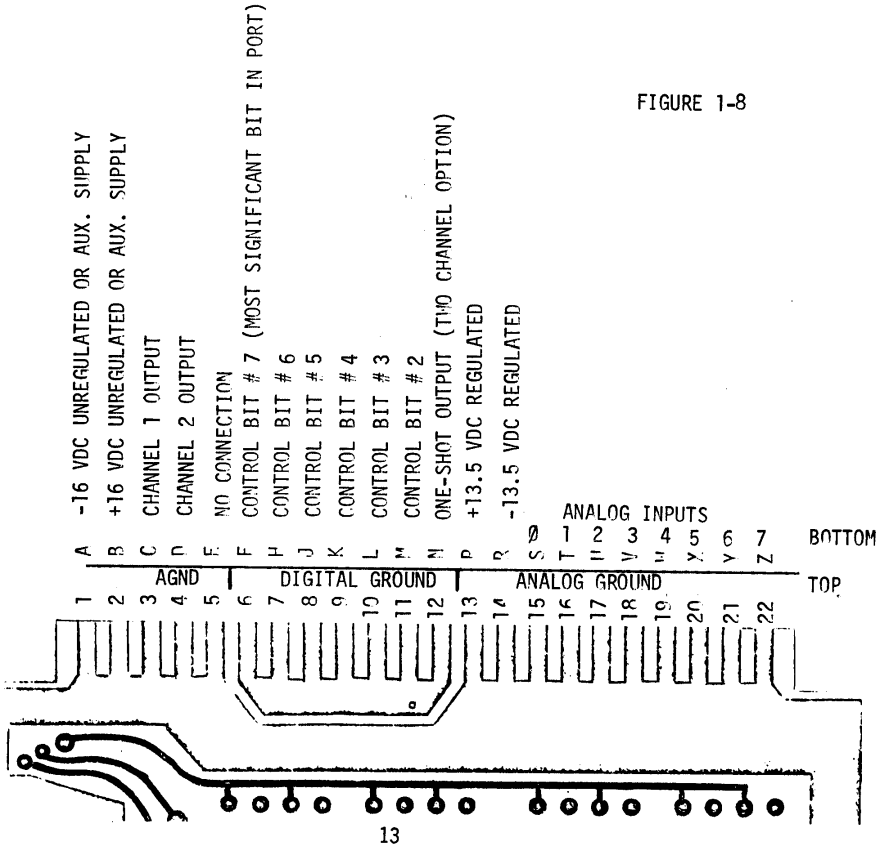


Figure 1-7

1.5 Hookup Requirements

The output of the A/D D/A interface is contained on the standard 44 pin edge connector located on the upper right hand corner of the board. The pinout of this connector is as shown in figure 1-8. It is strongly recommended that all the analog inputs and outputs be connected with low impedance coaxial cable to the back panel connector. The digital control outputs can be hooked up with twisted pairs or ribbon cable. If ribbon cable is used, it is recomended that every other conductor be tied to the digital ground opposite each control output. The back panel connector can be configured as desired, typically using the TRW connector DB-25S or equivalent.

FIGURE 1-8



2. Theory of Operation

2.1 Block Diagram

Shown in Figure 2-1 is the block diagram for the Analog Interface. This interface interacts with the Altair bus only upon specific input or output instructions. The board is assigned an eight bit address whose last two bits are ØØ. If an input or output instruction is directed at this address, then the address decoding and logic circuitry either enables the output driver or the registers. If it is an input instruction, then the driver puts the state of the eight analog comparators as a byte on the data in bus. If it is an output instruction, then the registers latch the data off the buffered data out bus. The contents of the registers form the inputs to the digital-to-analog converters (DAC'S) and the control outputs. Since only eight bits can be latched from the data bus at one time but 10 bits of analog resolution are desired, two bytes of data are used to form the input for each analog channel. Thus the registers are organized as four outputs ports, one for each state of the last two bits of the output port address.

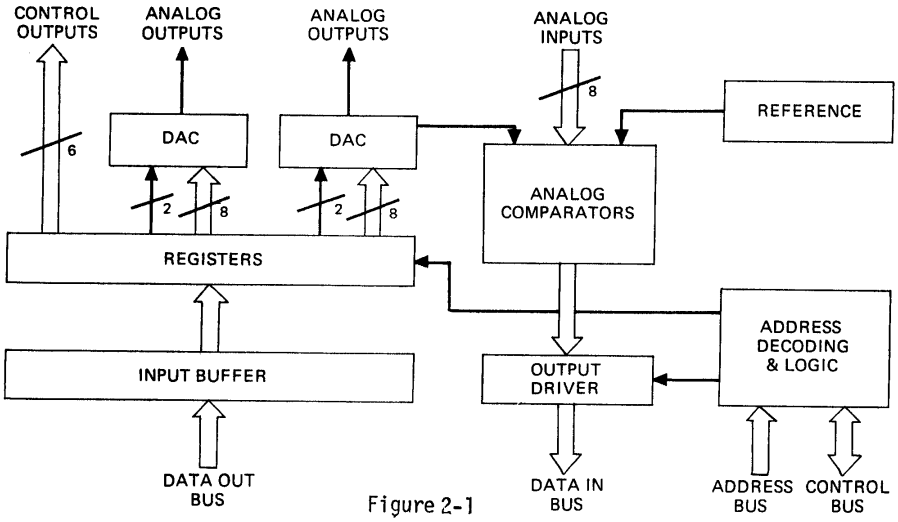
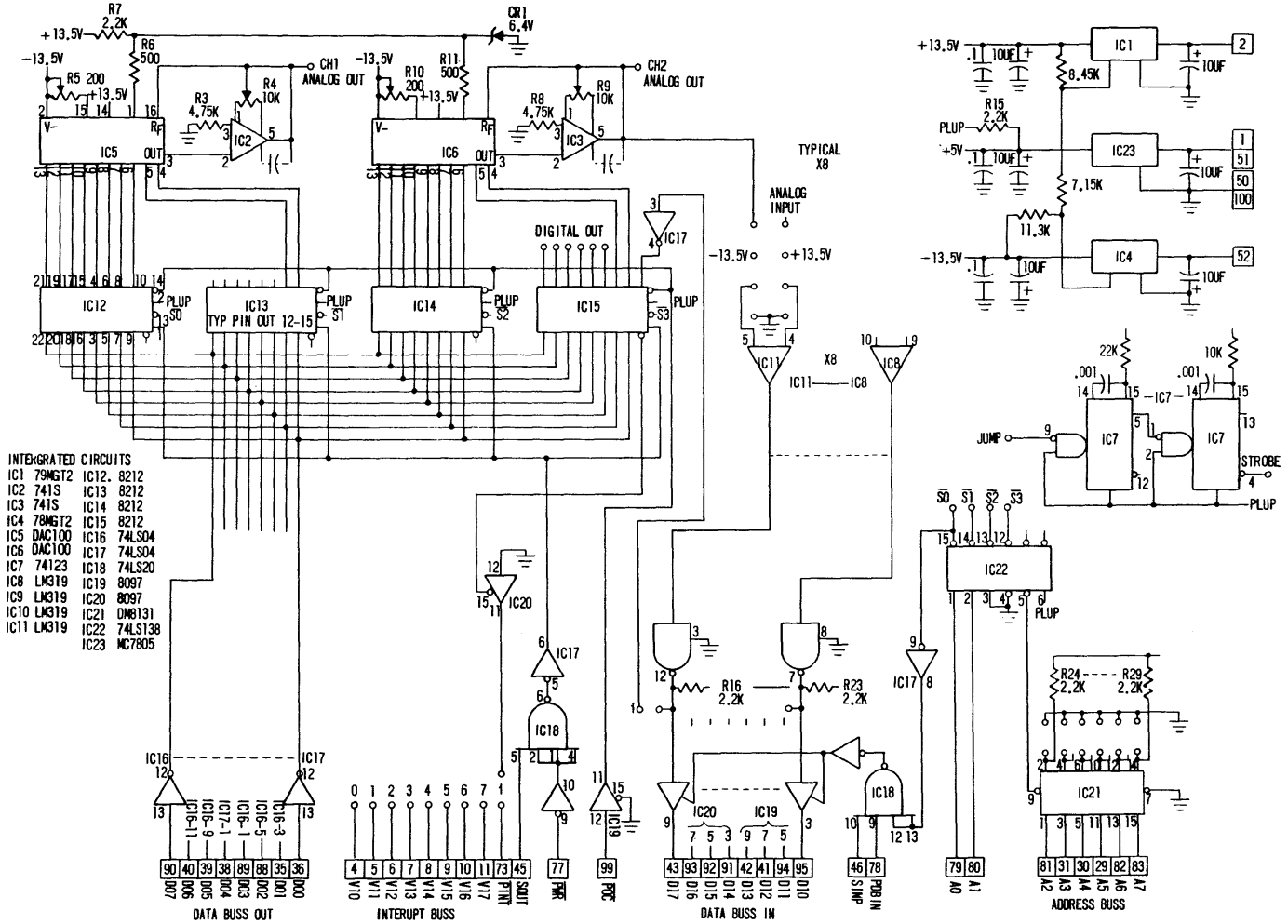


Figure 2-1

2.2 Schematic

The schematic for the Analog interface is shown in Figure 2-2. In the lower right hand corner the DM8131 six bit comparator checks the six most significant bits of the port address against the address bus, and if they match the comparator output enables the decoder (74LS138). The decoder then enables one of the four chip select lines (SØ, S1, S2, S3) depending on the state of the last two bits of address. The state of the control bus is decoded to determine whether an input or output instruction has been executed. If it is an input instruction, then the 8T97's are enabled to drive the data bus in with the state of the eight comparators. If it is an output instruction, then the 8212's are enabled so the selected chip (from SØ, S1, S2, or S3) will latch the data from the data bus out. The latched data then forms the digital input to the DAC's, which convert the digital information to an analog current flow via a laser-trimmed resistor network. The output current is then matched to the current flow through a bias resistor on the DAC by the 741SCP1 op amp, producing the voltage output. The 200Ω trimpot provides scale adjustment, and the 500 Ω or 10K trimpot (for bipolar or unipolar, respectively) allows for zero adjustment.


INTEGRATED CIRCUITS
IC1 79MGT2 IC12. 8212
IC2 741S IC13 8212
IC3 741S IC14 8212
IC4 78MGT2 IC15 8212
IC5 DAC100 IC16 74LS04
IC6 DAC100 IC17 74LS04
IC7 74123 IC18 74LS20
IC8 LM319 IC19 8097
IC9 LM319 IC20 8097
IC10 LM319 IC21 DM8131
IC11 LM319 IC22 74LS138
IC23 MC7805
DATA BUSS OUT
INTERUPT BUSS
DATA BUSS IN
ADDRESS BUSS
ANALOG INPUT
DIGITAL OUT
TYPICAL X8
CH1 ANALOG OUT
CH2 ANALOG OUT
JUMP
STROBE
PLUP

3. Application Notes

3.1 Point and Line Plotting on Scope

Point plotting on an oscilloscope can be achieved by connecting the two analog output channels to the vertical and horizontal inputs of the scope. The Z axis (beam intensity) can then be driven by the output strobe one-shot (section 1.3.5). In many cases this TTL output will drive the Z axis directly, but if more voltage is required a 7406 inverter can be used. The x and y values can be set into the registers by the appropriate output instructions, and the one-shot input can be selected to trigger upon the last instruction of the sequence. The dual one-shot waits for the output to settle for some 3μS and then plots the point.

Line plotting requires the use of sample and hold circuits to retain the x and y coordinates of the endpoints. A circuit such as shown in Figure 3-1 should be provided for each of the two channels. Once again the sample pulse can be provided by the output strobe one-shot.

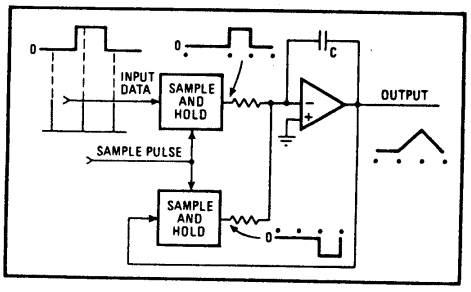


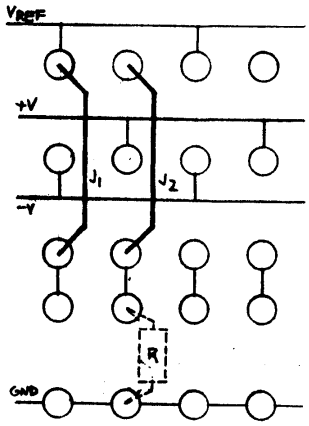
Figure 3-1

3.2 Plotter Interface

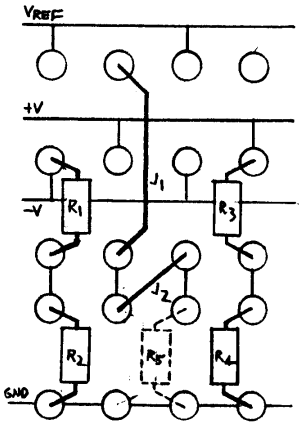
The x and y channels of an analog plotter can be driven directly with the error signals triggering the interrupt to minimize the software overhead. This allows the processor to perform other tasks while the plotter is in transit to the desired output state. When this point is achieved, an interrupt is generated and the next point is output. The error signals from the servos should be connected as null detectors as shown in Figure 3-2.

3.3 A/D Conversion Routines

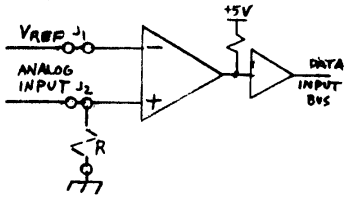
Attached are several analog-to-digital conversion routines in assembly code form. When mask bits are specified, this means that a binary one in a particular bit position selects that particular comparator as shown in Figure 1-3.

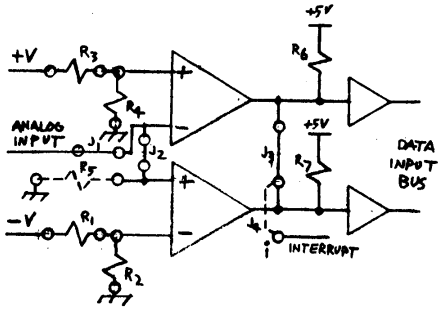


A/D CONVERSION OR
PROGRAMMABLE LIMIT SENSOR



NULL
DETECTOR





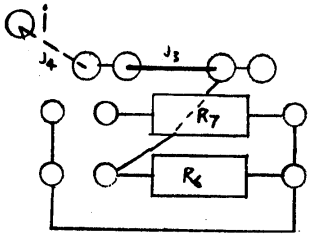


Figure 3-2

SUCCESSIVE APPROXIMATION

ANALOG TO DIGITAL CONVERSION PROGRAM

INP. PARAM.: Reg. C contains channel selection mask bits

OUT. PARAM.: Reg. E contains current value of analog input conversion time 247.5-340 S

```
ADC  :  XRA A   ; initialize approximation
        MOV E,A ; and counter
        STC
ADC1 :  RAR     ; rotate counter
        RC      ; return if done
        MOV D,A ; save counter
        ORA E   ; or with approx.
        OUT DAC ; send to DAC
        MOV E,A
        IN COMP
        ANA C   ; Check if   input
        MOV A,D ; restore counter
        JNZ ADC1;   input?
        XRA E   ; no,
        MOV E,A ; restore approx.
        MOV A,D ; restore counter
        JMP ADC1;
```

(23 BYTES)

10-BIT SUCCESSIVE APPROXIMATION

ANALOG TO DIGITAL CONVERSION

INP. PARAM.: C contains mask to select channel

OUT. PARAM.: H & L contain digital value of converted voltage

```
ADC:    LXI H,Ø  ; initialize approx.
        MOV D,H
        MOV E,L  ; initialize counter
        STC
ADC1:   MOV A,D
        RAR
        MOV D,A
        MOV A,E
        RAR
        MOV E,A
        ANI CØH  ; last bit?
        RNZ      ; yes, return
        ORA L
        MOV L,A
        OUT LDAC
        MOV A,D
        ORA H
```

10-BIT SUCCESSIVE APPROXIMATION (Cont.)

```
        MOV H,A
        OUT HDAC
        IN C
        JNZ ADC1
        MOV A,D
        XRA H
        MOV H,A
        MOV A,E
        XRA L
        MOV L,A
        JMP ADC1
```

8-CHANNEL TRACKING ADC PROGRAM

INP. PARAM.: Reg. H&L contain table address

OUT. PARAM.: Memory locations table to table +7 contain data for channels Ø-7 conversion time for 8 Ch. - 347.5-427.5 S

```
TADC :  XRA A    ;  reset counter
        STC
TADC1:  RAL      ;  rotate counter
        RC       ;  exit if done
        MOV D,A  ;  save counter
        MOV A,M  ;  get last valve
        OUT DAC  ;  set DAC
        INP COMP
        ANA D    ;  select channel
        JZ TADC2 ;  Vdac  Vsig?
        INR M    ;  no,
        INR M    ;  increment value
TADC2:  DCR M    ;  or decrement
        INX H    ;  increment table addr.
        MOV A,D  ;  restore counter
        JMP TADC1
```

(22 BYTES)

4. Specifications

D/A SECTION

RESOLUTION:	10 bits
LINEARITY:	0.2% max.
FULL SCALE:	10.0 V or ±5 V
CODE:	Offset binary
SLEW RATE:	10 V/ S min.
OUTPUT IMPEDANCE:	75 @ 20 KHz

COMPARATORS

NO. CHANNELS:	8
VOLTAGE OFFSET:	10 mV max.
VOLTAGE RANGE:	±10 V

A/D SECTION

METHOD:	Software controlled (drivers incl. for tracking and successive approx. converion)
RESOLUTION:	10 bits
FULL SCALE:	0-10 V or ±5 V
CONVERSION TIME:	Successive approx 350 S max tracking 50 S max per channel

STORAGE TEMPERATURE:	-25 to +85 C
OPERATING TEMPERATURE:	5-60 C
HUMIDITY:	0-95% non-condensing
QUIESCENT POWER REQUIREMENTS:	+15 to 18V @ 80 mA -15 to -18V @ 50 mA
BUS PENOUT:	Plug compatible with Altair 8800 bus
EDGE CONTACTS:	Gold plated, 100 pin (dual 50)on .125 centers
ANALOG CONNECTOR:	Gold plated edge contacts for 44 pin (dual 22) on .156 centers
DIMENSIONS:	%.0" x 10.0" (12.8 x 25.4 cm)

PLEASE NOTE

This manual has been carefully checked for accuracy, but no warranty is made as to the correctness of this document or the suitability of this product for any particular purpose. No liability is assumed for any damages, consequential or otherwise, that result from the use or misuse of this product.

WARRANTY

KIT: Defective parts will be replaced free of charge if returned to the factory within ten (10) days of receipt of delivery or upon written statement by purchaser that the unit was unassembled or untested for some longer period due to circumstances beyond his control. Completed units returned under similar circumstances will be repaired at a labor cost of $20/hr., with defective parts replaced free.

THE WARRANTY IS VOID IF THE KIT IS SOLDERED WITH CORROSIVE FLUX.

ASSEMBLED: The assembled units are fully warranted to be free of defects for ninety (90) days from the time of shipment. If they are found to be defective in this period they may be returned to the factory for repair or replacement free of charge (including return shipping).

POLYMORPHIC SYSTEMS
P. O. BOX 2207
GOLETA, CA 93018

PRELIMINARY

LOADING DIP (DUAL IN-LINE PACKAGE) DEVICES

Most DIP devices have their leads spread so that they can not be dropped straight into the board. They must be "walked in" using the following procedure;

(1) Orient the device properly. Pin 1 is indicated by a small embossed dot on the top surface of the device at one corner. Pins are numbered counterclockwise from pin 1.

(2) Insert the pins on one side of the device into their holes on the printed circuit card. Do not press the pins all the way in, but stop when they are just starting to emerge from the opposite side of the card.

(3) Exert a sideways pressure on the pins at the other side of the device by pressing against them where they are still wide below the bend. Bring this row of pins into alignment with its holes in the printed circuit card and insert them an equal distance, until they begin to emerge.

(4) Press the device straight down until it seats on the points where the pins widen.

(5) Turn the card over and select two pins at opposite corners of the device. Using a fingernail or a pair of long-nose pliers, push these pins outwards until they are bent at a 45 degree angle to the surface of the card. This will secure the device until it is soldered.